REMARKS

Election/restrictions:

The applicant respectfully traverse the restriction on the grounds that all claims pertain to programmable interconnect structures used to couple nodes in integrated circuits, and they describe procedures to establish the connection. Programmable circuits are used in these interconnect structures to allow a user to either couple or decouple nodes that are physically adjacent or apart from each other. In the programmable circuit, a first state allows for the coupling of two nodes, and a second state allows for the decoupling of the two nodes. Furthermore, the applicant discloses compact and fast switches. The applicant believes that the six independent claims are variants of such compact switches reasonable for a single prosecution. The six amended independent claims are listed below:

1. A programmable interconnect structure to couple a first node to a second node for an integrated circuit comprising:
a pass-gate fabricated on a substrate layer to electrically connect said first node to said second node; and
a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and
a programmable method to select between isolating said first and second nodes and connecting said first and second nodes by changing data stored in said memory bit.

6. A programmable interconnect structure to couple a first node to a second node for an integrated circuit comprising:
a power voltage and a ground voltage; and
a pull-up circuit coupled between said power voltage and said second node; and
a pull-down circuit coupled between said ground voltage and said second node; and
a programmable circuit coupled to said first node and to each of said pull-up and pull-down circuits; and
a configuration circuit including at least one memory element coupled to said programmable circuit, wherein altering the data in said at least one memory element provides a programmable method of:
decoupling said first node from second node by deactivating both said pull-up and pull-down circuits; and
coupling said first node to second node compelled by activating said pull-up and pull-down circuits.

22. A programmable interconnect structure to couple a first node to a second node for an integrated circuit comprising:
a wire having a first end and a second end; and
a first programmable interconnect structure as in claim 6, the first node of said first claim

6 structure coupled to said first node and the second node of said first claim 6 structure coupled to said first end of wire; and

a second programmable interconnect structure as in claim 6, the first node of said second claim 6 structure coupled to said second node and the second node of said second claim 6 structure, coupled to said second end of wire; and

a programmable method of coupling said first node to the wire by coupling said first claim 6 structure, and coupling said second node to the wire by coupling said second claim 6 structure; and

a programmable method of decoupling said first and second nodes from the wire by decoupling both of said first and second claim 6 structures.

27. A programmable interconnect structure to couple a plurality of first nodes to a plurality of second nodes for an integrated circuit comprising:

a first side comprising each of said first nodes wherein said structure originates and a second side comprising each of said second nodes wherein said structure terminates; and

a plurality of programmable interconnect structures as stated in claim 22, each said claim 22 structure further comprising:

the first node of claim 22 structure coupled to a first node at said first side with said structure wire having the first end at said first side; and

the second node of claim 22 structure coupled to a second node at said second side with said structure wire having the second end at said second side.

37. A programmable interconnect structure to couple a first node to a second node for an integrated circuit comprising:

a wire having a first end and a second end; and

a first programmable interconnect structure as in claim 30, the first node of said first claim 30 structure coupled to said first node and the second node of said first claim 30 structure coupled to said first end of wire; and

a second programmable interconnect structure as in claim 30, the first node of said second claim 30 structure coupled to said second node and the second node of said second claim 30 structure, coupled to said second end of wire; and

a programmable method of coupling said first node to second node by activating the first claim 30 structure pass-gate and deactivating the second claim 30 structure pass-gate, or by deactivating the first claim 30 structure pass-gate and activating the second claim 30 structure pass-gate.

43. A programmable interconnect structure for an integrated circuit comprising:

one or more pass-gates on a substrate layer to electrically connect two nodes; and

either a memory circuit or a conductive pattern in lieu of said memory circuit substantially above said pass-gates to control a portion of said pass-gates; and

an interconnect and routing layer substantially above said pass-gates to connect said pass-gates and one of said memory circuits and conductive pattern; and

a programmable method to select between isolating said first and second nodes

and connecting said first and second nodes by changing data either in the memory circuits or in the conductive pattern.

In Re. claims 1-5, the examiner noted that the claims fall under class 326, subclass 38. In claim 1, the applicant discloses an interconnect structure comprising a programmable pass-gate (also known as a switch) on a substrate layer, and a programming circuit including a memory element to control the switch (connection). The memory content allows the nodes to be connected or disconnected by controlling the switch. A first state of the configuration circuit connects the nodes, and a second state of the configuration circuit disconnects the node. When the nodes are disconnected, the second node is isolated from the first node, and has no coupling to the first node. This condition is also known as tri-stated in the IC literature. The ability to construct configuration circuit & memory elements above the switch offers the advantage of building a cheaper & faster compact switch for programmable logic circuits. The novelty is in the use of this compact switch to connect two nodes. In the next paragraph, the applicant will show that this structure is similar to claim 6 structure, and the claim elements are reasonable to be presented in the same prosecution with those for claim 6 structure. Withdrawal of the claim 1 restriction, and those dependent thereupon (claims 2-5) is respectfully requested.

In Re. claims 6-21, the applicant discloses a second programmable interconnect structure comprised of a different switch from that stated in claim 1, wherein many elements are similar to both. In claim 6 structure, the programmable circuit includes a memory element to control the connection (switch), similar to claim 1 structure. This is a first basis to traverse the restriction for claim 1. The memory content allows the nodes to be coupled or decoupled by controlling the switch, similar to claim 1 structure. This is a second reason to traverse the restriction. The configuration circuit and memory element may be constructed above the programmable logic circuits to construct a compact switch, similar to the claim 1 structure. This is a third reason to traverse the restriction. This aspect of the compact switch structure is presented in the dependent claim 15 and claim 19. These overlapping similarities provide multiple reasons for the Applicant to present both independent claims in the current prosecution. The examiner noted that claim 6 falls under subclass 82 of current converting circuits. A fourth basis to traverse the restriction is that node 2 in claim 6 structure has no pre-requisite of requiring a high drive current. There is also no voltage conversion pre-requisite such as TTL to CMOS. The claim 6 structure comprises a different programmable circuit to achieve the same result as that in claim 1: to connect or

disconnect node 1 from node 2. The claim 6 structure provides extra advantages including of being able to use as a buffer structure with appropriate transistor sizing, as described in the body of the application on page 40. Without such transistor sizing, the claim 6 structure is simply another switch to couple a first node to a second node. The applicant used the terminology "buffer structure" to separate claim 1 structure from claim 6 structure for ease of language, without implying that node 2 mandates a higher current drive. Please note that the language has been corrected in the amended claim 6. Advantages in the claim 6 structure also includes the elimination of series resistance incurred with claim 1 structure, and the ability to couple a rejuvenated signal. The applicant respectfully submits that claim 1 structure fall under the same classification as claim 6 structure.

In Re. claims 30-38, the applicant discloses an extended claim 6 structure. This interconnect structure comprises a claim 1 and a claim 6 structure, both coupling the first node to the second node. There may be one configuration circuit for the integrated structure. In claim 30, the programmable circuit includes a memory element to control the connection (switch), similar to claim 1 & claim 6 structures. This is a first basis to traverse the restriction. The memory content allows the nodes to be coupled or decoupled by controlling the switch, similar to claim 1 & claim 6 structures. This is a second reason to traverse the restriction. The configuration circuit and memory element may be constructed above the programmable logic circuits, similar to the claim 1 & claim 6 structures. This is a third reason to traverse the restriction. These overlapping similarities provide multiple reasons to present claim 30 in the current prosecution. The examiner noted that claim 30 falls under subclass 82 of current converting circuits. A fourth basis to traverse the restriction is that node 2 in claim 30 structure has no pre-requisite of requiring a high drive current. The claim 30 structure comprises a different programmable circuit to achieve the same result as that in claim 1 and claim 6; namely it provides either a claim 1 structure to couple the nodes or a claim 6 structure to couple the nodes. The claim 6 structure portion may be used to eliminate series resistance, to couple a rejuvenated signal or as a buffer structure, with appropriate transistor sizing, as explained in the body of the application on page 40. Without such transistor sizing, the claim 30 structure is simply another switch to couple a first node (could be coupled to a first wire) to a second node (could be coupled to a second wire). The applicant used the terminology "buffer structure" to separate claim 1 structure from claim 6 structure for ease of language, without implying that node 2 mandates a high current drive.

Please note that the language has been corrected in the amended claim 6. The significant advantages with the claim 30 structure is that it allows a parallel connection with either a claim 1 structure, or a claim 6 structure. Withdrawal of the claim 30 restriction, and those further dependent thereupon (claims 31-36) is respectfully requested.

In Re. claim 22, the applicant discloses a structure to couple two nodes further apart in comparison to the claim 1 and claim 6 structures. The coupling comprises a wire that traverses some distance. The wire may be a short or a long one, and does not limit the claim to any specific loading restriction. The claim 22 structure comprises two claim 6 structures, and hence each switch is a very compact switch. This is a first reason to traverse the restriction. The two nodes are coupled to the wire by a first configuration state of the programmable circuits. This is similar to claim 1 and claim 6 structures, and a second reason to traverse the restriction. The two nodes are decoupled from one another and from the wire by a second configuration state of the programmable circuits, also similar to claim 1 and claim 6 structures. This is a third reason to traverse the restriction. In the restriction, the examiner sited that this claim falls under subclass 83, or of field-effect transistor. There is no unipolar action of FETs associated with the claim, and this is a fourth reason to traverse the restriction. The claim 22 structure, comprises a plurality of claim 6 structures and a wire, and has no FET type source/drain current requirement. The current may flow from node 1 to node 2 or visa-versa. Similar to claim 6 structure there is also no restriction on wire loading or current drives as required in subclass 82. Withdrawal of the claim 22 restriction, and those dependent thereupon (claims 23-26) is respectfully requested.

In Re. claim 27, the applicant discloses a structure to couple a plurality of nodes at one end to a plurality of nodes at another end, the two ends further apart in comparison to the claim 1 and claim 6 structures. The coupling comprises a plurality of wires that traverses some distance. Each wire may be a short or a long one, and does not limit the claim to any specific loading. A first node is coupled to a second node by a claim 22 structure; hence this is an extension of claim 22 to a plurality of such structures. This is a first reason to traverse the restriction. Said two nodes are coupled to the wire by a first configuration state of the programmable circuits. This is similar to claim 1, claim 6 and claim 22 structures, and a second reason to traverse the restriction. Said two nodes are decoupled from one another and from the wire by a second configuration state of the programmable circuits, also similar to claim 1, claim 6 and claim 22 structures. This is a third reason to traverse the restriction. In the restriction, the examiner sited

that this claim falls under subclass 83, or of field-effect transistor. There is no unipolar action of FETs in the claim, and this is a fourth reason to traverse the restriction. The claim 27 structure, comprises a plurality of claim 22 structures, each said claim 22 structure comprising a plurality of claim 6 structures, and there is no FET type source/drain current requirement. Withdrawal of the claim 27 restriction, and those dependent thereupon (claims 28-29) is respectfully requested.

In Re. claims 23-26, 28, 29, 39-42, the examiner has sited that the claims fall under class 326, subclass 47. Under subclass 47, there is an emphasis for the claim elements to fall into significant design emphasis on the topological arrangement of components and their circuit connectors. All the listed claims describe interconnect structures connecting or coupling nodes. They all have a configuration circuit. A first state of the configuration circuit connects nodes, similar to claim 1, claim 6, claim 22, claim 27 and claim 30 structures. This is a first reason to traverse the restriction. A second state of the configuration circuit disconnects nodes, similar to claim 1, claim 6, claim 22, claim 27 and claim 30 structures. This is a second reason to traverse the restriction. The configuration circuit in all the claims can be in full or in part be constructed above the logic elements to construct compact switches, similar to claim 1, claim 6, claim 22, claim 27 and claim 30 structures. This is a third reason to traverse the restriction. All of the listed claims are a combination of claims 1, 6, 22, 27, 30 that the applicant has previously stated to be of similar content for this prosecution, and hence a fourth reason to traverse the restriction. The applicant does not present a specific layout configuration for the restricted claim elements, which is a fifth reason to traverse the restriction. In each restricted claim element, only the configuration circuit including the memory element is similarly located as in claim 1, 6, 22, 27 and 30 structures. The configuration circuit is positioned above the substrate layer where the logic transistors are located to construct the compact switch. The configuration circuit can be distributed across the entire IC and coupled to the logic circuits. The connection of nodes is accomplished through the switch; as stated in claim 1, 6, 22, 27, 30. The circuit connectors of these switches to each other and other input/output nodes have no topological restrictions or preferences. This is a sixth reason to traverse the restriction. Withdrawal of all restrictions (claims 23-26, 28, 29, 39-42) is respectfully requested.

In Re. claim 37-42, the applicant discloses a structure to couple two nodes further apart in comparison to the claim 1 and claim 6 structures. The coupling comprises a wire that traverses some distance. The wire may be a short or a long one, and does not limit the claim to any

specific loading restriction. The structure comprises a plurality of claim 30 structures. This is a first reason to traverse the restriction. The two nodes are coupled to the wire by a first configuration state of the programmable circuits. This is similar to claim 1 and claim 6 structures, and a second reason to traverse the restriction. The two nodes are decoupled from one another and from the wire by a second configuration state of the programmable circuits, also similar to claim 1 and claim 6 structures. This is a third reason to traverse the restriction. The switch can be made very compact, similar to claim 1 and claim 6 structures, a fourth reason to traverse the restriction. In the restriction, the examiner sited that this claim falls under subclass 82, or of a current driving device. There is no restriction for the claim 37 structure to be a current driving device. This is a fifth reason to traverse the restriction. The claim 37 structure, comprises a plurality of claim 30 structures, further comprising a plurality of claim 1 and claim 6 structures. When two claim 1 structures at either end are coupled to the wire in the middle, the two claim 6 structures are deactivated. Withdrawal of the claim 37 restriction, and those dependent thereupon (claims 38-42) is respectfully requested.

In Re. claim 43, the applicant discloses a programmable interconnect structure similar to the claim 1 and claim 6 structures. The claim 43 structure further comprises the ability to have either a memory circuit, or a metal pattern in lieu of the memory circuit as the configuration circuit to connect two nodes. The interconnect structure is invariant to the choice of the configuration circuit. Similar to claim 1 & claim 6 structures, a first state of the configuration circuit couples the nodes, a first basis to traverse the restriction. A second state of the configuration circuit decouples the nodes, a second basis to traverse the restriction. The configuration circuit (both options) is positioned above the switch transistor to form a compact and fast switch, similar to claim 1 and claim 6 structures, a third basis to traverse the restriction. The examiner noted that the claims 43-48 falls under class 716, subclass 16. The applicant respectfully submits that the amended claims place the claim 43 structure in the same class as the claim 6 structure requested for the current prosecution. Withdrawal of the claim 43 restriction, and those dependent thereupon (claims 44-48) is respectfully requested.

The examiner omitted claim 48 in the office action. The applicant assumes that claim 48 was placed under category V in the examiner's response.

CONCLUSION

The applicant believes that the above submission is fully responsive to the office action.

If for any reason the Examiner believes that a telephone conference would in any way expedite this matter, the Examiner is invited to telephone the Inventor Mr. Madurawe at (408) 737-8868 or on his cell phone at (408) 431-5367.

Respectfully submitted,

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Applicant